

IN THE CLAIMS:

Please amend claims 1, 2, 7-9, 11, 12, 16, 17, 20, 21, and 26-28, and please add new claims 30-43, as set forth below.

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1 (Currently Amended) A method comprising:
2 initializing a circuit said circuit having at least one memory element coupled to a
3 memory bus on a host system;
4 monitoring signals on the memory bus;
5 detecting a first sequence of signals, the first sequence of signals including a
6 reserved memory address; and
7 switching control of the at least one memory element to the circuit in response to
8 detection of the first sequence of signals. *(via an arbiter)*

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1 2. (Currently Amended) The method of claim 1 further comprising:
2 detecting a second sequence of signals, the second sequence of signals including
3 another reserved memory address; and
4 switching control of the at least one memory element to the host system in
5 response to detection of the second sequence of signals.

1 3. (Original) The method of claim 2 wherein error correcting codes are switched off
2 prior to switching control of the at least one memory element to the host system.

4. (Original) The method of claim 1 wherein initializing a circuit having at least one memory element coupled to a memory bus on a host system comprises detecting a sequence of writes to memory locations on the circuit.

5. (Original) The method of claim 4 wherein the sequence of writes are writes to random memory locations on the circuit.

6. (Original) The method of claim 1 wherein monitoring signals on the memory bus comprises the circuit monitoring control, address, and data signals on the host system.

7. (Currently Amended) The method of claim 1 wherein detecting a first sequence of signals comprises detecting at least one write signal to ~~a particular memory location on the circuit~~ the reserved memory address.

8. (Currently Amended) The method of claim 1 wherein detecting a first sequence of signals comprises detecting at least one read signal from ~~a particular memory location on the circuit~~ the reserved memory address.

9. (Currently Amended) The method of claim 1 wherein switching control of the memory bus to the circuit comprises a processing element in the circuit reading from or writing to the at least one memory element in the circuit.

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1 10. (Original) The method of claim 2 wherein switching control of the at least one
2 memory element to the host system comprises a processor on the host system reading
3 from or writing to the at least one memory element.

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1 11. (Currently Amended) An apparatus comprising:
2 a memory bus on a host system;
3 a plurality of memory elements on a circuit, said plurality of memory elements
4 communicatively coupled with the memory bus;
5 a processing element on the circuit communicatively coupled with the plurality of
6 memory ~~element~~ elements and the memory bus, said processing element to
7 monitor signals on the memory bus;
8 detect a first sequence of signals, the first sequence of signals including a reserved
9 memory address; and
10 switch control of the plurality of memory elements to the circuit in response to
11 detection of the first sequence of signals.

1 12. (Currently Amended) The apparatus of claim 11 further comprising said
2 processing element to detect a second sequence of signals, the second sequence of signals
3 including another reserved memory address; and
4 switch control of the plurality of memory elements to the host system in response to
5 detection of the second sequence of signals.

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1 13. (Original) The apparatus of claim 12 wherein error correcting codes are switched
2 off prior to switching control of the plurality of memory element to the host system.

1 14. (Original) The apparatus of claim 11 wherein the processing element is at least
2 one of a field programmable gate array, and a processor.

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1 15. (Original) The apparatus of claim 11 wherein the processing element to monitor
2 signals on the memory bus comprises the processing element to monitor control, address,
3 and data signals on the host system.

1 16. (Currently Amended) The apparatus of claim 11 wherein the processing element
2 to detect a first sequence of signals comprises the processing element to detect at least
3 one write signal to a particular memory element on the circuit the reserved memory
4 address.

1 17. (Currently Amended) The apparatus of claim 11 wherein the processing element
2 to detect a first sequence of signals comprises the processing element to detect at least
3 one read signal to a particular memory element on the circuit the reserved memory
4 address.

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1 18. (Original) The apparatus of claim 11 wherein the processing element to switch
2 control of the plurality of memory element to the circuit comprises the processing
3 element reading from or writing to the plurality of memory elements.

1 19. (Original) The apparatus of claim 12 wherein the processing element to switch
2 control of the plurality of memory elements to the circuit comprises a processor on the
3 host system reading from or writing to the plurality of memory elements.

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1 20. (Currently Amended) An article of manufacture comprising:
2 a machine-accessible medium including instructions that, when executed by a
3 machine, causes the machine to perform operations comprising
4 initializing a circuit said circuit having at least one memory element coupled to a
5 memory bus on a host system;
6 monitoring signals on the memory bus;
7 detecting a first sequence of signals, the first sequence of signals including a
8 reserved memory address; and
9 switching control of the at least one memory element to the circuit in response to
10 detection of the first sequence of signals.

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1 21. (Currently Amended) The article of manufacture as in claim 20, further
2 comprising instructions for detecting a second sequence of signals, the second sequence
3 of signals including another reserved memory address; and
4 switching control of the at least one memory element to the host system in response to
5 detection of the second sequence of signals.

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1 22. (Original) The article of manufacture as in claim 21, further comprising
2 instructions for switching of error correcting codes prior to switching control of the at
3 least one memory element to the host system.

1 23. (Original) The article of manufacture as in claim 20, wherein said instructions for
2 initializing a circuit having at least one memory element coupled to a memory bus on a
3 host system comprises further instructions for detecting a sequence of writes to memory
4 locations on the circuit.

1 24. (Original) The article of manufacture as in claim 23, wherein said instructions for
2 detecting a sequence of writes include further instructions for writing to random memory
3 locations on a circuit.

1 25. (Original) The article of manufacture as in claim 20, wherein said instructions for
2 monitoring signals on the memory bus comprises further instructions for the circuit
3 monitoring control, address, and data signals on the host system.

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1 26. (Currently Amended) The article of manufacture as in claim 20, wherein said
2 instructions for detecting a first sequence of signals comprises further instructions for
3 detecting at least one write signal to a ~~particular memory location on the circuit~~ the
4 reserved memory address.

1 27. (Currently Amended) The article of manufacture as in claim 20, wherein said
2 instructions for detecting a first sequence of signals comprises further instructions for
3 detecting at least one read signal from a ~~particular memory location on the circuit~~ the
4 reserved memory address.

1 28. (Currently Amended) The article of manufacture as in claim 20, wherein said
2 instructions for switching control of the memory bus to the circuit comprises further
3 instructions for a processing element in the circuit reading from or writing to the at least
4 one memory element in the circuit.

1 29. (Original) The article of manufacture as in claim 21, wherein said instructions for
2 switching control of the at least one memory element to the host system comprises further
3 instructions for a processor on the host system reading from or writing to the at least one
4 memory element

1 30. (New) The method of claim 1, wherein the reserved memory address corresponds
2 to a reserved address in the at least one memory element in the circuit.

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1 31. (New) The method of claim 1, wherein the reserved memory address corresponds
2 to a reserved address in a second memory coupled with the memory bus.

1 32. (New) The apparatus of claim 11, wherein the reserved memory address
2 corresponds to a reserved address in the plurality of memory elements of the circuit.

1 33. (New) The apparatus of claim 11, wherein the reserved memory address
2 corresponds to a reserved address in a second memory coupled with the memory bus.

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1 34. (New) The article of manufacture of claim 20, wherein the reserved memory
2 address corresponds to a reserved address in the at least one memory element in the
3 circuit.

1 35. (New) The article of manufacture of claim 20, wherein the reserved memory
2 address corresponds to a reserved address in a second memory coupled with the memory
3 bus.

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1 36. (New) A method comprising:
2 monitoring signals on a memory bus, the memory bus coupled with a memory and
3 a first processor; and
4 in response to detecting a reserved memory address on the memory bus, switching
5 control of the memory from the first processor to a second processor coupled with the
6 memory bus.

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1 37. (New) The method of claim 36, further comprising:
2 in response to detecting another reserved memory address on the memory bus,
3 switching control of the memory from the second processor to the first processor.

1 38. (New) The method of claim 36, wherein the reserved memory address
2 corresponds to a reserved address in the memory.

1 39. (New) The method of claim 36, wherein the reserved memory address
2 corresponds to a reserved address in a second memory coupled with the memory bus.

1 40. (New) The method of claim 36, wherein detecting the reserved memory address
2 comprises detecting one of a read to the reserved memory address and a write to the
3 reserved memory address.

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41. (New) The method of claim 36, wherein the memory and the second processor
comprise part of a single component.

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42. (New) The method of claim 41, wherein the single component comprises a dual
inline memory module (DIMM) coupled with the memory bus.

43. (New) The method of claim 36, wherein the memory comprises a synchronous
dynamic random access memory (SDRAM).